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09/834,408	04/13/2001	Lawrence T. Clark	42390P11097	3613

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	3

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/834,408	Applicant(s) CLARK ET AL.	
	Examiner Suresh K Suryawanshi	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-23 are presented for examination.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Specification

3. The disclosure is objected to because of the following informalities: no application number is provided at page 2, line 5.

Appropriate correction is required.

4. Claim 8 is objected to because of the following informalities: need to delete either "the" or "a" at page 15, line 9. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 7-18 and 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimoto (US Patent no 6,256,252 B1).

7. As per claim 1, Arimoto teaches

a first circuit adapted to store a volatile logic value [fig. 1; col. 1, line 65 – col. 2, line 6; col. 9, line 64 – col. 10, line 3; memory circuit]; and

a second circuit adapted to generate a logic value, wherein the integrated circuit is adapted to decouple a power supply potential from at least a portion of the second circuit in a first operational mode [fig. 1; col. 1, line 65 – col. 2, line 6; col. 9, line 64 – col. 10, line 3; power supply to logic circuit is stopped in the standby state of memory-embedded LSI; col. 1, lines 16-21; memory-embedded LSI formed by a logic circuit and memory circuit on the same semiconductor substrate].

8. As per claim 2, Arimoto teaches that the integrated circuit further comprises a coupling transistor to couple and decouple the second circuit from the power supply potential [fig. 33; col. 24, lines 16-21; power supply switching transistor 114].

9. As per claim 3, Arimoto teaches that the coupling transistor is in series between the second circuit and a node to be couple to the power supply potential [fig. 33].

10. As per claim 7, Arimoto teaches that the integrated circuit further comprises a voltage regulator and the integrated circuit is adapted to couple the first circuit to the voltage regulator in the first operational mode [fig. 1; VDDM].

11. As per claim 8, Arimoto teaches that the integrated circuit is adapted to decouple a power supply potential from the first circuit when in a second operational mode [col. 13, lines 4-7].

12. As per claim 9, Arimoto teaches that the second circuit is adapted to generate the logic value based at least in part on the volatile logic value [col. 10, lines 60-67].

13. As per claim 10, Arimoto teaches that the integrated circuit is further adapted to couple the first circuit and the second circuit to the power supply potential in a second operational mode [inherent to the system to provide the power supply to both logic circuit and memory circuit during non standby mode].

14. As per claim 11, Arimoto teaches that the integrated circuit is further adapted to couple the first circuit and the second circuit to each other in the second operational mode [col. 1, lines 18-21; fig. 1].

15. As per claim 12, Arimoto teaches decoupling a power supply voltage potential from a logic circuit while retaining a volatile logic value in a memory circuit when an integrated circuit is in a first operational mode [fig. 1; col. 1, line 65 – col. 2, line 6; col. 9, line 64 – col. 10, line 3; power supply to logic circuit is stopped in the standby state of memory-embedded LSI and retaining a volatile logic value in the memory circuit; col. 1, lines 16-21; memory-embedded LSI formed by a logic circuit and memory circuit on the same semiconductor substrate].

16. As per claim 13, Arimoto teaches coupling the logic circuit and the memory circuit to the power supply voltage potential when the integrated circuit is in a second operational mode [inherent to the system to provide the power supply to both logic circuit and memory circuit during non standby mode].

17. As per claim 14, Arimoto teaches coupling the logic circuit to the memory circuit [col. 1, lines 18-21; fig. 1].

18. As per claim 15, Arimoto teaches coupling the memory circuit to a voltage regulator when the integrated circuit is in the first operational mode [fig. 1; VDDM].

19. As per claim 16, Arimoto teaches generating a logic value with the logic circuit based, at least in part, on a volatile logic value stored in the memory circuit when the integrated circuit is in a second operational mode [col. 10, lines 60-67].

20. As per claim 17, Arimoto teaches

a static random access memory [col. 4, line 53; SRAM]; and

an instruction processing unit [fig. 1; col. 4, line 8; semiconductor integrated circuit device], the instruction processing unit comprising:

a first circuit to store a volatile logic value [fig. 1; col. 1, line 65 – col. 2, line 6; col. 9, line 64 – col. 10, line 3; memory circuit]; and

a second circuit to generate a logic value [fig. 1; col. 1, line 65 – col. 2, line 6; col. 9, line 64 – col. 10, line 3; power supply to logic circuit is stopped in the standby state of memory-embedded LSI; col. 1, lines 16-21; memory-embedded LSI formed by a logic circuit and memory circuit on the same semiconductor substrate].

21. As per claim 18, Arimoto teaches that the instruction processing unit further comprises a coupling transistor to couple and decouple the second circuit from the power supply potential [fig. 33; col. 24, lines 16-21; power supply switching transistor 114].

22. As per claim 20, Arimoto teaches that the instruction processing unit is adapted to couple the first circuit to the voltage regulator in the first operational mode [fig. 1; VDDM].

23. As per claim 21, Arimoto teaches that the instruction processing unit is adapted to decouple a power supply potential from the first circuit when in a second operational mode [col. 13, lines 4-7].

24. As per claim 22, Arimoto teaches that the instruction processing unit is further adapted to couple the first circuit and the second circuit to the power supply potential in a second operational mode [inherent to the system to provide the power supply to both logic circuit and memory circuit during non standby mode].

25. As per claim 23, Arimoto teaches that the instruction processing unit is further adapted to couple the first circuit and the second circuit to each other in the second operational mode [col. 1, lines 18-21; fig. 1].

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 4-6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto (US Patent no 6,256,252 B1).

28. As per claims 4, 5 and 19, Arimoto discloses the invention substantially. Arimoto does not disclose expressly about a logic transistor having a gate dielectric layer that is thinner than a gate dielectric layer of the coupling transistor. However, a routineer in the art would know the use of thinner transistors in a logic circuitry as naturally this will allow more transistors to be fit within the same amount of area on a semiconductor die. But at same time, one will keep the coupling transistor to the power supply potential thicker as to prevent current leakage. Therefore, it would have been obvious to one of ordinary skill in the art to have a logic transistor having a gate dielectric layer that is thinner that a gate dielectric layer of the coupling transistor.

29. As per claim 6, Arimoto discloses the invention substantially. Arimoto does not disclose about a pass transistor. However, it is well known in the art to employ a pass transistor logic circuit to reduce a number of elements and power consumption, and to improve operating speed. Therefore, it would have been obvious to one of ordinary skill in the art to use a pass transistor in parallel with the coupling transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

sks
December 10, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100